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Immittance response of $CaSnO_3$ prepared by self-heat-sustained reaction

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The potential of $CaSnO_3$ for application as a capacitor component possessing a small temperature coefficient of capacitance has been examined by ac small-signal measurements at elevated temperatures (25–300 °C) in the frequency range 5–13 MHz. The samples were synthesized by a novel technique called self-heat-sustained (SHS) reaction. The ac data were acquired for the $CaSnO_3$ samples sintered at various temperatures with varying soak temperatures, T, and some times, t (1200 °C $\leq T \leq$ 1600 °C; 2 h $\leq t \leq$ 48 h). An analysis of the electrical data in more than one complex-plane formalism indicated relaxation processes. The resistance of these sintered samples was dominated by the grain boundaries, and the capacitance exhibited near-linear behavior at elevated temperature for several decades of measurement frequency. The electrical behavior has been correlated with the evolved microstructure in these samples in conjunction with the results obtained in a previous study for solid-state reaction (SSR) derived sintered bodies. The multi-plane analytical criteria provided a meaning for the lumped equivalent circuit representation including the origin and purpose of the contributing elements extracted from each complex plane formalism.

1. Introduction

The ac small-signal electrical characterization and subsequent analysis by the lumped parameter/complex plane (LP/CPA) technique of sintered $CaSnO_3$ synthesized via the conventional solid-state reaction (SSR) technique has recently been reported [1]. This analytical approach revealed that the capacitance of the resulting sintered body remained invariant over several decades of frequency in addition to a very weak temperature dependence in the range 25–300 °C. An average value of 2–3 pF and 3–7 pF over the same measurement temperature range was assigned to $CaSnO_3$ sintered at 1200 and 1350 °C, respectively. In the present investigation, the ac small-signal electrical response of $CaSnO_3$ derived from a novel synthesis technique, known as the self-heat-sustained (SHS) reaction [2] is reported. There are two reasons for adopting multiple synthesis processes: (1) availability of limited information in the literature and only the SSR route was mentioned in reference [3], and (2) to determine the most favorable synthesis technique in terms of the phase purity and benign microstructure in the sintered bodies with desired electrical behavior.

Since these devices are prepared from the polycrystalline materials, it is important to understand the contributions of grains, grain boundaries and other phases including physically distinct regions in the microstructure. Thus, a correlation among the processing, resulting microstructure, and total electrical behavior of these materials is warranted. Such a correlation is not adequately addressed in the recent literature [3], wherein the variation of capacitance and dielectric loss in the temperature range of 27–227 °C at three spot frequencies (1, 10, and 100 kHz) only have been reported. Moreover, the samples used in these studies were sintered at a single temperature for one soak time. The results obtained in these studies are, therefore, not likely to be representative of the true behavior of the material investigated.

In this work the ac small-signal response of $CaSnO_3$ sintered at various temperature (T) and soak time (t) profiles, in the frequency domain 5 Hz–13 MHz has been evaluated in the temperature range 25–300 °C. The objective is to assess an overall electrical response including the magnitude of the temperature dependence of the capacitance. The ac small-signal electrical data were analyzed via the lumped parameter/complex plane analysis (LP/CPA) technique to unravel the underlying competing phenomena operative within the complex microstructures. This approach is well known in the

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literature as immittance (impedance/admittance) spectroscopy (IS). The LP/CPA technique has proven to be a useful means of characterizing the electrical nature of a number of polycrystalline heterogeneous materials and devices [4–12]. An application of such a technique reveals the degree of structural uniformity, variation in electrical conduction path, stability, degradation, time-dependent processes, etc. in the potential materials or device systems.

2. Experimental procedure

2.1. Material synthesis

The samples investigated in this work were synthesized via a novel reaction technique, viz. the self-heat-sustained (SHS) reaction. In this synthesis metallic tin powder (99.999% powder, Pi-Kem, Surrey, UK) was mixed with $Ca(NO_3)_2 \cdot 4H_2O$ (98%, Fluka, UK) in a 1:1 molar ratio. The mixture was placed in an alumina boat and first heated slowly to and maintained at 250 °C for 4 h so as to facilitate complete melting of metallic tin (m.p. = 232 °C). The temperature was then raised monotonically to 800 °C and maintained for another 4 h to cause the reaction between molten and free-flowing tin and $Ca(NO_3)_2$. The mixture was finally calcined at 1100 °C for 12 h and then at 1200 °C for 24 h. The temperature was monitored by placing a K-type thermocouple close to the reaction zone ascertaining the occurrence of an SHS reaction. An X-Y recorder connected to the thermocouple indicated the self-heat-sustained reaction at its onset. An analysis of the powder X-ray diffraction (XRD) pattern of the resulting material confirmed the formation of $CaSnO_3$ as a single phase. This pattern was also used to detect the presence of any unreacted starting materials and/or new Ca or Sn-rich phases.

The calcined powder (obtained above via the SHS technique) was blended with 10 wt % polyvinyl alcohol (PVA) as binder, dried under an ultraviolet lamp and pressed into pellets (6 mm in diameter and 1–2 mm in thickness) by uniaxial pressing at a pressure not exceeding 100 MPa. The use of PVA is a common practice in the sintering of electroceramic bodies, which provides strengthening and lubrication effects so that the particles remain closer to one another. Such an effect assists in achieving higher densities in sintered bodies than those sintered without the binder. The choice of PVA in this work was due to its relatively easier combustion kinetics compared to those of polyethylene glycol (PEG).

The as-pressed pellets were sintered at three different temperatures (T), viz. at 1200, 1350 and 1600 °C, for soak times (t) varying from 2 h to 48 h in air. It was presumed that the selection of a wide temperature-time (T-t) profile would provide an understanding of the material behavior via resulting microstructures and controlled properties better than that reported previously [3]. The slice samples prepared from these sintered discs were used in the electrical measurements.

The granular features of the starting $CaSnO_3$ powder as well as the sintered discs were monitored by using a JEOL-6400SM (Japan) scanning electron microscope (SEM). Elemental identification and subsequent quantification at various regions of the sintered samples were accomplished by using the energy dispersive spectroscopy (EDX) analyzer (Link eXL, UK) attached to the above SEM. Due to the strong susceptibility toward moisture, the calcined powder as well as the sintered discs were stored in a humidity-free bottle containing anhydrous $CaCl_2$ except where used for measurement purposes.

2.2. Preparation of measurement samples and mounting

Small slice samples taken from the sintered pellets were coated with silver paint on opposite parallel faces (Electrolube Ltd., UK) and cured at 500 °C for 2 h. The thicknesses of the slice samples prepared for electrical measurements was kept identical. Such a sample was placed between two highly polished stainless steel discs serving as electrodes mounted on Perspex walls. Thus, the sample was fitted securely with adjustable screws on both sides of the holder provided by HP (Hewlett-Packard) accessories. This arrangement allowed better sample-holding capability with an ohmic contact with resistance less than 2 Ω.

For the acquisition of ac data at elevated temperatures (25–300 °C), a custom designed "all stainless steel" sample holder was mounted on an alumina brick ($25 \times 25 \times 10$ mm^3). To ensure good adherence, high-temperature alumina cement was used and cured at 225 °C for 30 min. Each sample was introduced into the uniform temperature zone of a custom-designed small, low-thermal mass, precalibrated horizontal furnace with temperature fluctuations not more than 1 °C. The furnace was heated to the desired temperature, at a constant incremental rate of 10 °C min^{-1}. Adequate time was allowed for equilibration at the measurement temperature within the sample before the acquisition of ac electrical data.

2.3. Electrical measurements

The ac small-signal electrical data on the sintered samples were acquired as a function of applied measurement frequency in the range 5 Hz–13 MHz using a HP4192A LF Impedance Analyzer (Yokogawa, Japan). Fully automated experimental control was achieved via a desktop PC as the instrument controller. The small-signal amplitude was about 1 V and the acquired ac data were reproducible within the small variation of this signal voltage. These data were analyzed using a proprietary software package [13] which allowed automated data acquisition in any of the desired forms, such as, impedance, admittance or phasor, as a function of frequency. Further, this software was capable of analysing the ac electrical data in all four complex plane formalisms including Bode plane analysis [7–10]. Necessary electrical parameters were extracted from these representations which employed a non-linear least-squares curve-fitting (CNLS) procedure [4–10, 13, 14]. This extraction procedure does not assume or simulate any equivalent circuit configuration *a priori*, which is often the case with commercial software.

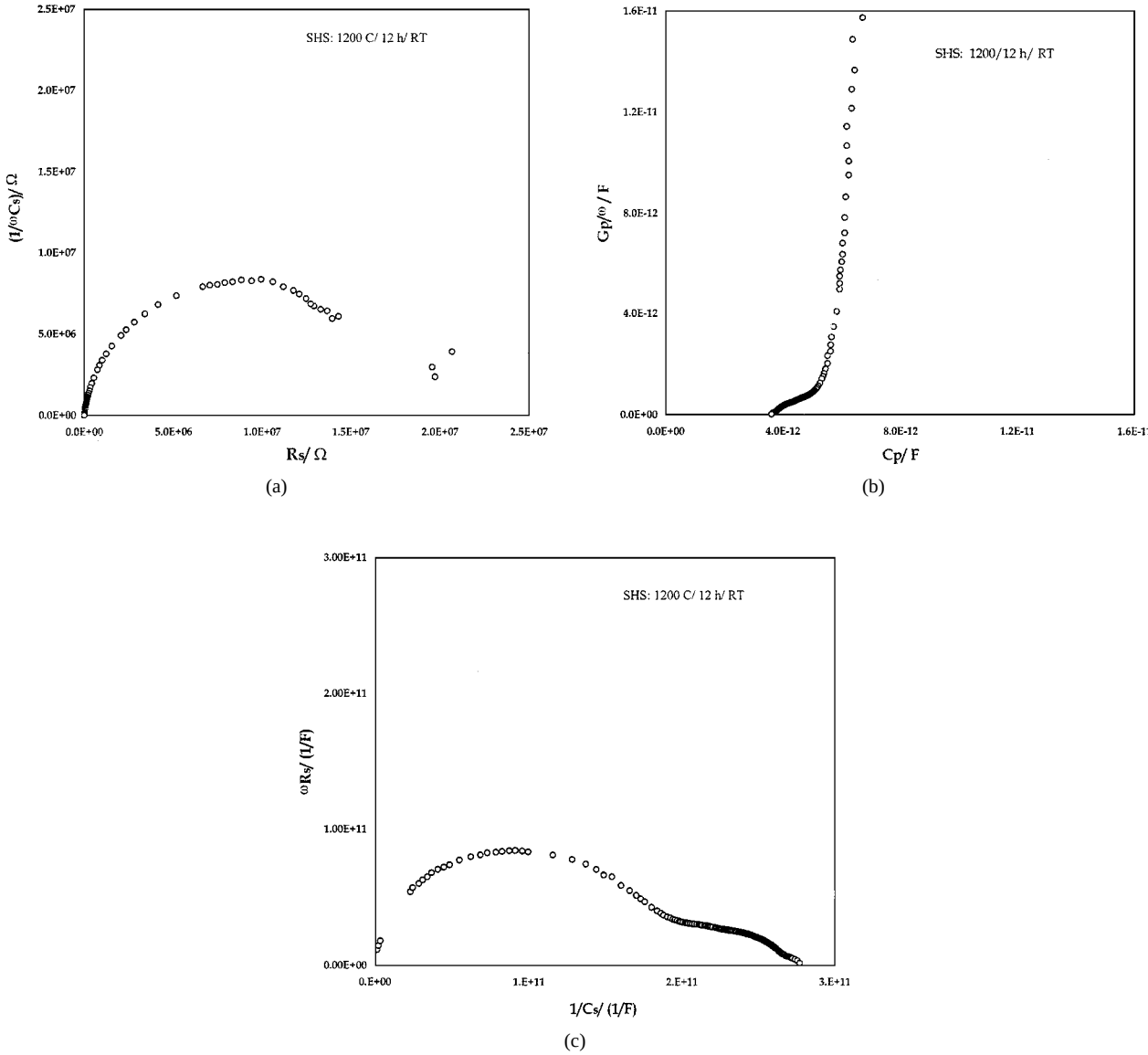


Figure 1 Room-temperature complex plane plots for the sample sintered at 1200 °C for 12 h (a) Impedance (Z^*) plot, (b) complex capacitance (C^*) plot, and (c) modulus (M^*) plot of the same data.

3. Results and discussion

The overall electrical behavior of the SHS derived $CaSnO_3$ material is identical to the SSR derived samples reported earlier [1]. Accordingly, the analysis of the acquired ac data utilizing four complex planes in the temperature range 25–300 °C revealed semicircular relaxation(s) in the impedance (Z^*), complex capacitance (C^*), and modulus (M^*) planes for all the SHS samples investigated. There was no meaningful feature of the as-acquired data in the admittance (Y^*) plane. The multi-plane analytical criteria have provided maximum information [7–12] for an unknown materials system. Such an analytical approach provides more insight into the material system for appropriate engineering applications. The general features of the ac data included (a) a single-like semicircular relaxation in the Z^*-plane, (b) a semicircle in the high-frequency region including a vertical line parallel to the imaginary (y-) axis in the low-frequency region in the C^*-plane, and (c) mostly a single-like but in some cases overlapped like-two semicircle in the M^*-plane.

The room temperature (25 °C) relaxation of the ac data is shown in Fig. 1a to c for the samples sintered at 1200 °C for 12 h. Fig. 1a reveals the lumped total resistance (R_{total}) of about 20.1 MΩ in the Z^*-plane, which matches well with the dc resistance (R_{dc}) of about 20 MΩ. The corresponding capacitance, C_{total}, has a value of about 7 pF extracted from the peak frequency ($\omega R_{\text{total}} C_{\text{total}} = 1; \omega = 2\pi f = 1/\tau$, where τ is the time constant (or relaxation time) of the semicircular relaxation in the Z^*-plane. The individual contributions of the grains and the grain-boundaries could not be deconvoluted even at elevated temperatures in the Z^*-plane. When the same ac data are displayed in the C^*-plane (Fig. 1b), the terminal capacitance neatly resolved into three distinct components:

(a) segment of the vertical line parallel to the imaginary axis at low frequencies,

(b) high-frequency semicircular arc, having a right-intercept on the real axis at a point approximately lying on the extrapolation of the straight line, and

(c) a finite left-intercept (an intercept on the left-hand side of the semicicrcular relaxation on the real axis) at high-frequencies.

The finite left-intercept, C_2, was found to be about 3.6 pF. Further evaluation of the semicircular relaxation between the high frequency capacitance and the straight line segment yielded the total capacitance ($C_{\text{total}} = C_1 + C_2$) as about 7.7 pF. This is close to what is obtained in Z*-plane. The capacitance C_1 (about 4.1 pF) extracted from the semicircular relaxation (Fig. 1b) is the trapping capacitance, which is a series event with the corresponding resistance ($R_1 =$ 3.9 MΩ). These trapping elements (C_1 and R_1) are not treated in the same way as in ZnO-based varistor materials [6, 15] because of their lower sensitivity as a function of ambient temperature. This lower sensitivity is one of the reasons to obtain the temperature coefficient of capacitance (TCC) of the sintered $CaSnO_3$ bodies.

The terminal admittance at ultra-low frequencies (i.e. near the dc limit) appears to be dominated by the dc conductance in the C*-plane. Such a cut-off response was previously seen in ZnO-based varistors [6]. It is, therefore, reasonable to assume that the imaginary part of C* approached infinity asymptotically at a finite out-of-phase component ($C_{\text{total}} = C_1 + C_2$) value which can be considered as a near-static (dc) capacitance as the frequency approached zero.

The finite left-intercept (C_2) represents a lumped capacitance response of the barrier layer effect originating at the grain-boundary regions and of the single crystal-like behavior of the lumped grains. Therefore, C_2 is a parallel combination of two capacitances: (1) lumped grain-boundary capacitance, and (2) lumped grain capacitance. A comparison of the relative magnitudes of the lumped grains and grain-boundary capacitance indicates that the contribution of the lumped grains constituting C_2 is likely to be small compared to the barrier layer effect at the grain-boundaries. Thus, the geometric capacitance originating from the grain boundary depletion regions associated with the barrier layer is the dominating component within C_2, which in turn can be referred to as the barrier layer capacitance. C_2 is predominantly determined by a 'trap-free' contribution at the depletion region across the grain-boundaries due to its origin in the high-frequency domain. This depletion region can be regarded as an "electrical thickness" which sustains the major portion of the applied electrical field from the signal voltage under non-equilibrium conditions. Thus, the electrical field drop across the lumped grains is much smaller than the electrical field drop across the lumped grain-boundary electrical thickness. The large dc conductivity attributed to the donors within the lumped grains is responsible for the small electrical field drop. Thus the single-crystal-like dielectric behavior of the lumped grains mentioned earlier is incorporated into C_2.

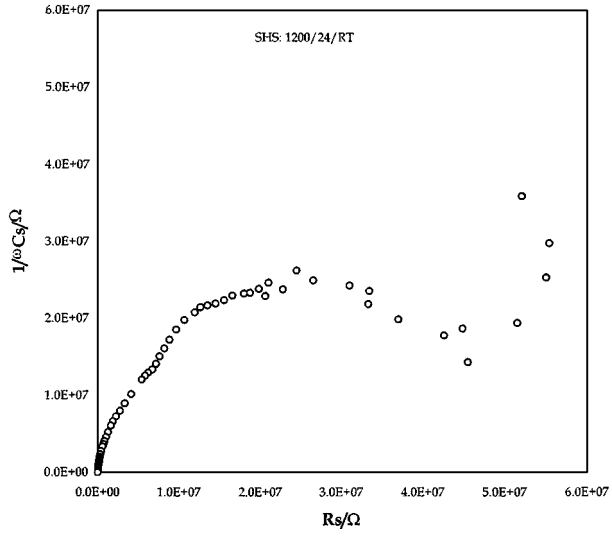
The C*-plane relaxation does not give directly the grain bulk resistance (R_g) and the grain boundary resistance (R_{gb}). However, these two resistances lump together to form a total resistance ($R_{\text{total}} = R_1 + R_2$) which is the dc resistance (R_{dc}) and influences the asymptotic behavior as the frequency approaches zero. Since the same data exhibit relaxation processes in more than one complex plane, this dual relaxation is attributed to a set of parametric conditions used in the equivalent circuit elements outlined by Seitz [16]. Thus, the purpose of the multiplane analytical technique approach advocated in [7–10] is conductive to the understanding of the complex material system.

Further examination of the same data in the M*-plane (Fig. 1c) reveals two overlapping semicircular relaxations in the frequency domain. These two overlapped semicircles yielded values of 5.6 pF and 17 MΩ for C_{gb} and R_{gb} respectively, in the low-frequency domain. Combining this with the R_{total} of 20.1 MΩ from the Z*-plane (Fig. 1a), a value of 3.1 MΩ for R_g could be computed. The capacitance 5.6 pF is somewhat higher than found in the C*-plane. This is because C_{gb} is influenced by the grain capacitance (C_g) in the form of a series lumped-component attached to it when the trapping capacitance is not isolated.

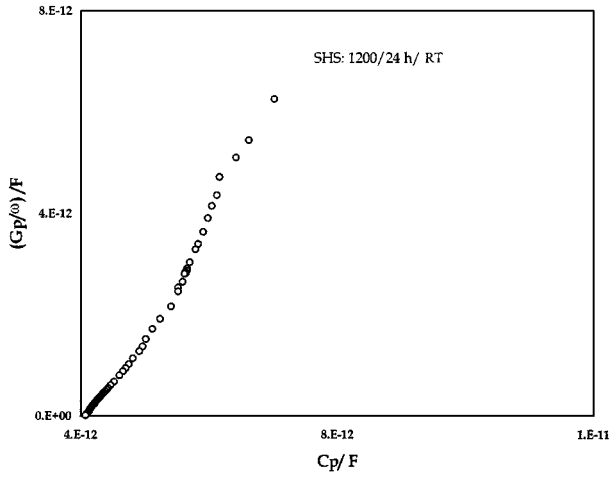
The room temperature ac data for the sample, soaked at 1200 °C for 24 h, showed a single-like lumped behavior in the Z*-plane (Fig. 2a). The Z*-plane yielded a semicircle with left intercept on the real axis near to the origin (∼0). The right-intercept (intercept on the right-hand side of the semicircular relaxation) is the chord length in this case, which can be interpreted as the total resistance, R_{total}, and is found to be approximately 80 MΩ. The corresponding lumped capacitance (C_{total}) is computed to be 8.5 pF. The M*-plane analysis yielded R_g as 32 MΩ and C_{total} as 4 pF. Thus, $R_{gb}(= R_{\text{total}} - R_g)$ becomes 48 MΩ. When the same data were displayed in the C*-plane (Fig. 2c), the finite left-intercept (C_2) on the real axis was found to be about 4.1 pF, which provides 8.9 pF for the total capacitance $C_{\text{total}}(=C_1 + C_2)$ when adding the trapping capacitance (C_1) obtained from the semicircular relaxation. This is close to the lumped value of 8.5 pF obtained in the Z*-plane.

A similar exercise with the room-temperature ac electrical data on the sample sintered at 1200 °C for 48 h, yielded a total resistance (R_{total}) of about 135 MΩ and total capacitance (C_{total}) of about 5.3 pF from the Z*-plane plot of Fig. 3a. Further calculation yielded 6.1 pF for C_g and 41.4 MΩ for R_g from this plot. Thus, R_{gb} is about 93.6 MΩ. The value of C_g corresponds to the dielectric constant ε_r of the single crystal of $CaSnO_3$ which is about 6 [$\varepsilon_r = (C/\varepsilon_o) \times (d/A)$, where C is the terminal capacitance, $\varepsilon_o = 8.854 \times 10^{-12}$ F m^{-1}, d is the thickness of the material (m) and A is the electrode cross-sectional area (m^2)]. This value is identical to that obtained in the case of SSR-derived $CaSnO_3$, sintered at 1200 °C for 24 h [1]. C_2 is extracted as 2.4 pF and $C_{\text{total}}(= C_1 + C_2)$ as 8.5 pF in the C*-plane using Fig. 3b.

It is seen from the above analyses that an increase in the soak time caused an increase in the total resistance ($R_{\text{total}} = R_{dc}$). This was about 20 MΩ for 12 h soak time, increasing to about 80 MΩ for 24 h soak time and then to about 135 MΩ for 48 h soak time.



(a)



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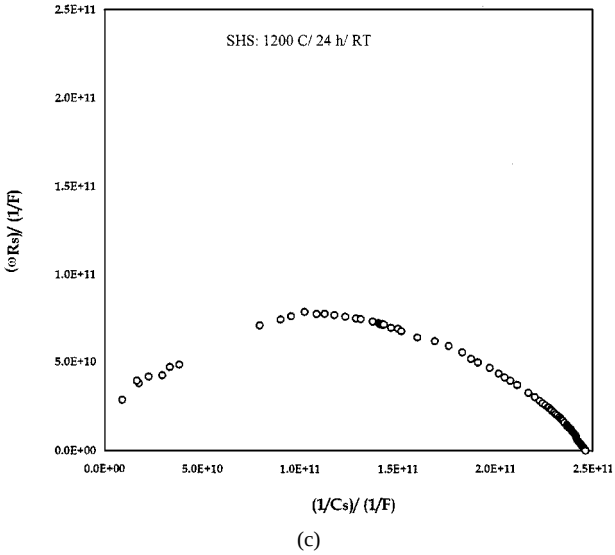
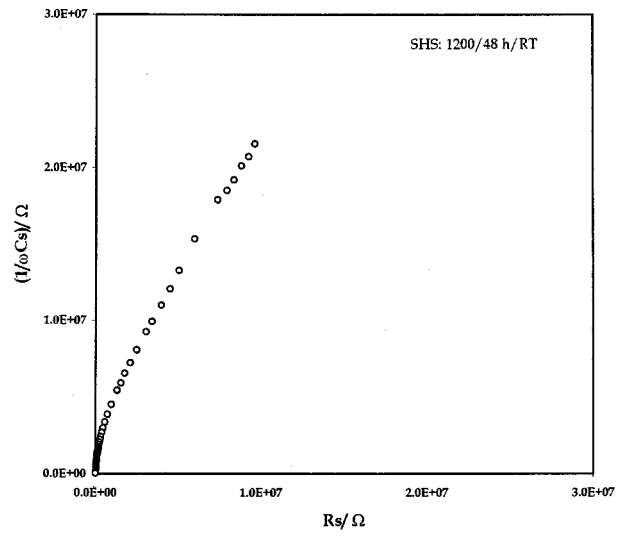


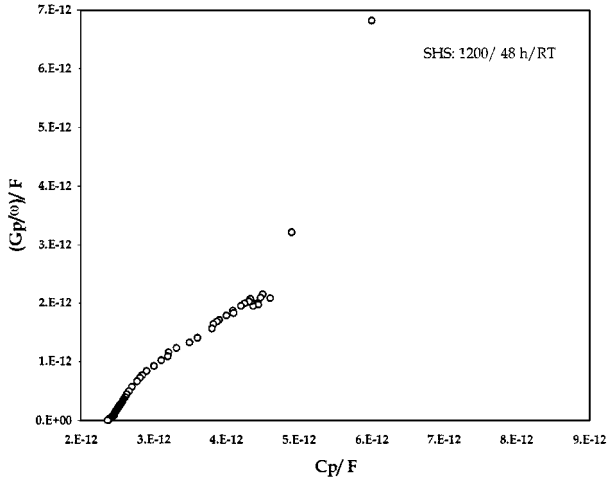
(c)

Figure 2 Room temperature complex plane plots for the sample sintered at 1200 °C for 24 h (a) Impedance (Z*) plot, (b) complex capacitance (C*) plot and (c) modulus (M*) plot of the same data.

Thus, the grain-boundary contribution ($R_{gb} = 17$ MΩ, 48 MΩ and 93.6 MΩ in the samples soaked at 1200 °C for 12 h, 24 h, and 48 h, respectively) is the major contribution to the total resistance. Such an enhancement in the resistance is possibly related to improved densification via better compaction of the grain-to-grain contact. The concept of compaction allows an improved uniformity in the grain size distribution when compared to the samples sintered at 1200 °C for 12 hours. Fig. 4 demonstrates these microstructural features.



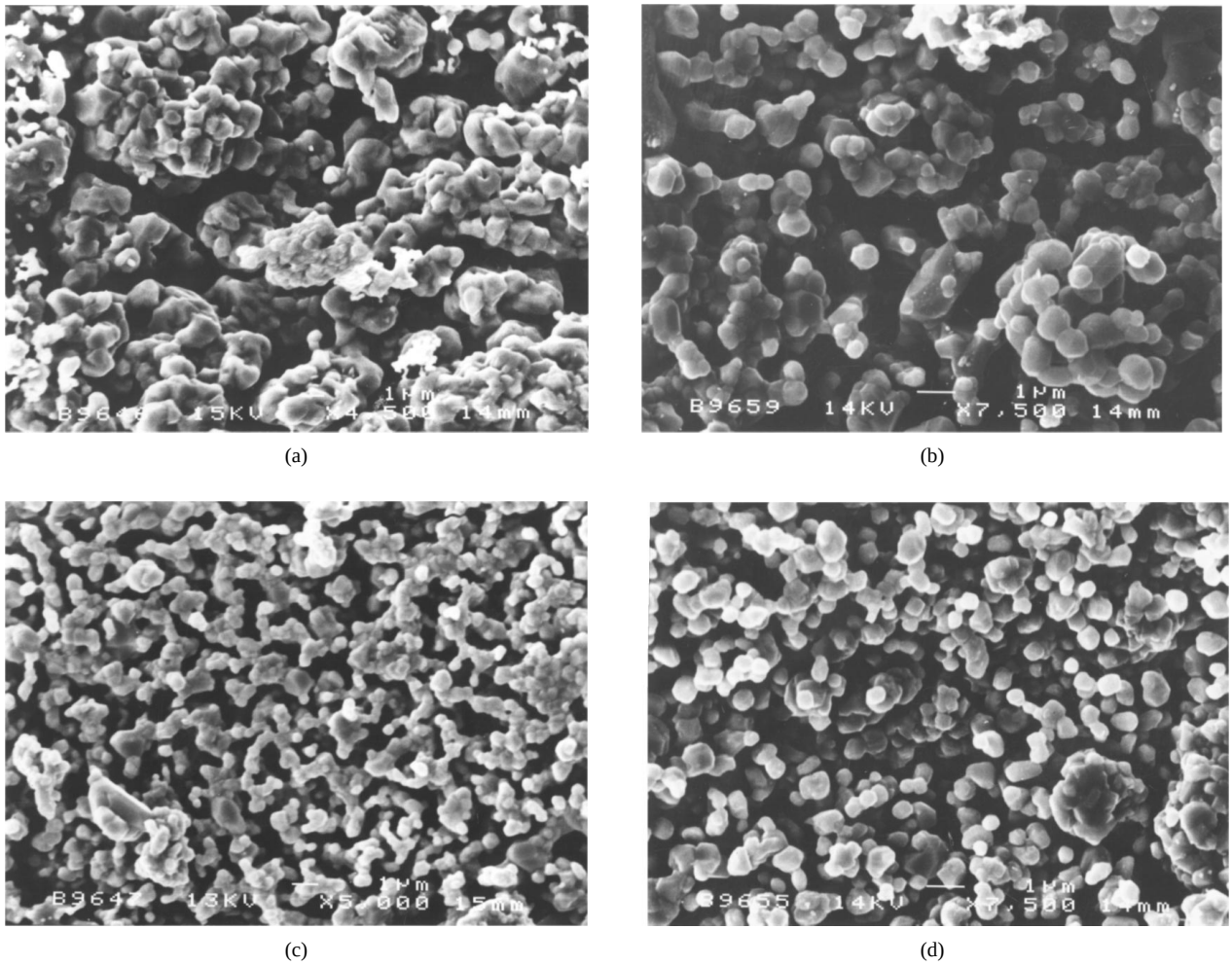
(a)



(b)

Figure 3 Room temperature complex plane plots for the sample sintered at 1200 °C for 48 h. (a) Impedance (Z*) plot and (b) complex capacitance (C*) plot for the same data.

It should be noted that sintering at 1200 °C did not cause significant grain growth (the average grain size was approximately 1 μm) as the soak time was increased from 12 to 48 h for the SHS samples. At these sintering profiles, more or less monosized grains with uniform grain-boundary demarcation regions were obtained. However, the densification of the sintered body improved systematically via the decrease in porosity and enhanced intergranular connectivity as the soak time of sintering increased. The porosity could not be eliminated completely even after 48 h soak time at 1200 °C. This is a major limitation in the SHS synthesis, causing a relatively higher degree of porosity in the resulting product. Nevertheless, about 95% of this porosity is open in nature, which can be eliminated during the sintering step, thereby leaving a dense and compact body [17–18]. This fact is very well substantiated in the microstructural evolution which is illustrated in Fig. 4.



(a) (b)

(c) (d)

Figure 4 Microstructural features of the $CaSnO_3$ samples sintered at 1200 °C for (a) 12 h, (b) 24 h (c) 36 h, and (d) 48 h.

Considering small capacitance values having a major fluctuation in these samples, it can be concluded that the degree of homogeneity or heterogeneity of the trap levels at the grain boundaries was nearly unaffected in samples soaked up to 48 h at 1200 °C. In each case, the lumped semicircular relaxations in the Z^* plane were depressed, i.e. the center of the semicircle lies below the x-axis, exhibiting a finite depression angle (θ). The amount of finite depression angle is akin to that observed in the case of SSR-derived $CaSnO_3$ material [1]. It is indicative of the distribution of the relaxation processes and termed as a non-Debye behavior of the material. This is also an indication of the degree of heterogeneity in the operative electrical paths across the sample. However, the small magnitude of θ (10°, 15° and 15° for samples sintered at 1200 °C for 12, 24, and 48 h, respectively) suggests that the degree of heterogeneity in the lumped electrical paths is nearly invariant with increasing soak time at a given sintering temperature.

The room-temperature ac electrical data for the samples sintered at 1350 °C for 24 h exhibited similar relaxations in the Z^*-, C^*- and M^*-planes, which are depicted in Fig. 5a to c. From these plots, R_{total} and C_{total} were found to be about 12.3 MΩ and 6.6 pF, respectively. The depression angle in the Z^* plane was about 11.1°. R_g was extracted as 7.2 MΩ with a corresponding C_g of about 4.7 pF. The grain-boundary resistance, $R_{gb}(= R_{total} - R_g)$, was computed as 5.1 MΩ. The finite left-intercept (C_2) in the C^*-plane plot was about 4.1 pF, and the trapping capacitance (C_1) was about 8.6 pF. The trapping resistance (R_1) was found to about 5.1 MΩ.

Two interesting features of the analyses provided here are worth mentioning. First, the total sample resistance decreased from about 80 MΩ (sintered at 1200 °C) to 12.3 MΩ (sintered at 1350 °C). The lumped grain-boundary resistance, nevertheless, was the dominant part of the total resistance. Second, the total capacitance remained almost invariant with the temperature of sintering (∼10–12 pF). This suggests that the total barrier layer thickness which is inclusive of the applied "electrical field experiencing region" (hereafter "electrical field falling region" as this region experiences a drop in the applied electrical field due to the associated resistance as it happens for a set of series resistors for a fixed applied voltage) within the sample is nearly invariant with the sintering temperature. In fact, the ac small-signal electrical field is distributed over this thickness within the sample as it refers to the highly resistive region that experiences a drop (or distribution) in the applied electrical field. Therefore, a term "electrical field falling region" for the resistive region of the barrier layer thickness is coined to illustrate the voltage distribution effect in the series-like set of resistors per Kirchoff's voltage law. Furthermore, this invariant

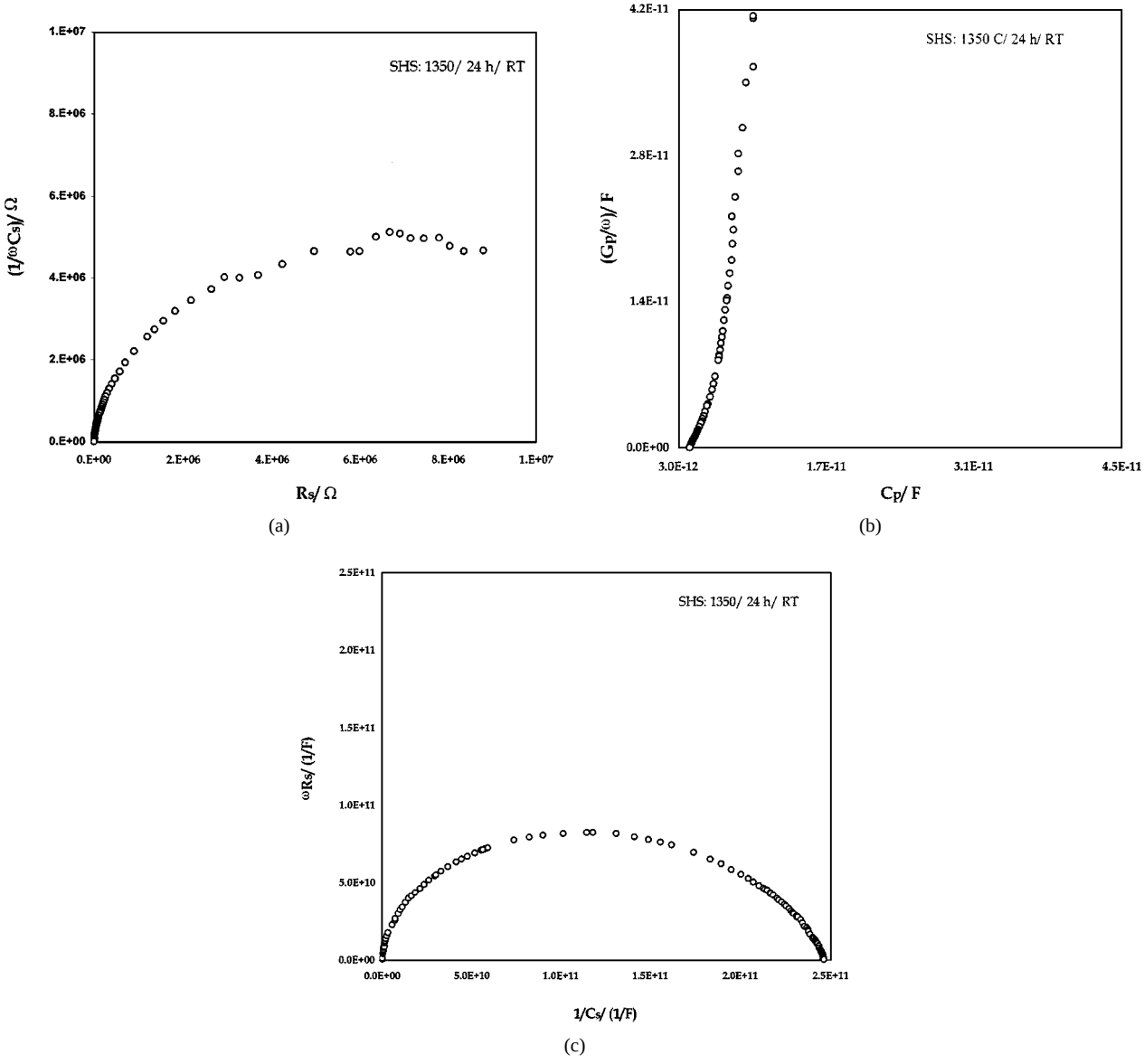


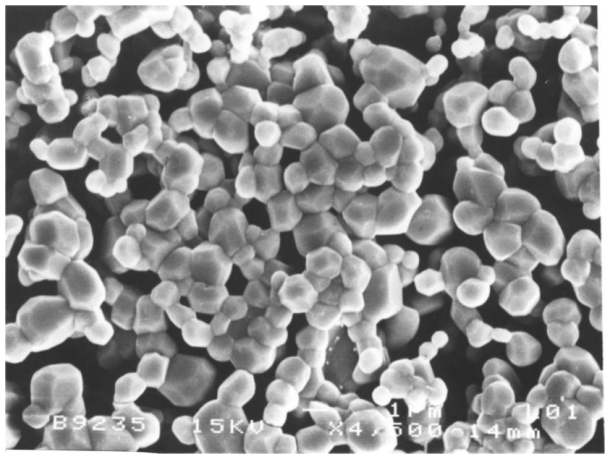
Figure 5 Room temperature complex plane plots for the sample sintered at 1350 °C for 24 h. (a) Impedance (Z*) plot, (b) complex capacitance (C*) plot, and (c) modulus (M*) plot of the same data.

trend implies that the nature of conduction mechanism, charge carriers, trapping parameters, etc. are not altered in these samples.

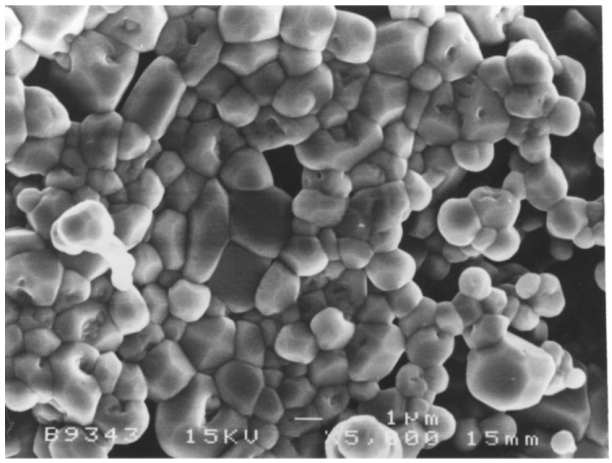
The room-temperature ac data for the samples sintered at 1350 °C for 48 h yielded single-like lumped relaxation in both Z*- and M*-planes. The relaxation in the C*-plane yielded a finite left-intercept followed by a single-like semicircle with a vertical line asymptotically parallel to the imaginary axis. The extracted circuit elements from the Z*-plane match very well with those from the M*-plane. These elements were further supported by the C*-plane analysis.

It is evident that the total resistance of the sample increased steadily as the soak time was increased from 24 to 48 h at 1350 °C. The grain-resistance remained nearly unaltered (∼7.2–7.9 MΩ). Accordingly, the lumped contribution of the grain-boundaries increased steadily (∼5–27.4 MΩ). The microstructural features of samples sintered at 1350 °C for 24 and 48 h are shown in Fig. 6a and 6b, respectively. There is an indication of reduced porosity in the samples sintered for longer soak times. This reduction is attributed to lack of grain growth and downsizing of the grain-size distribution. From the microstructural features, the majority of grains can be assigned a size of 1 μm. However, the density of the sintered bodies in the two samples is still far from ideal, considering the amount of porosity that still exists in both the samples. Nevertheless, as stated above, this porosity is open in nature and can be eliminated.

The circuit capacitance of the $CaSnO_3$ samples sintered at 1350 °C (soak time 24 to 48 h) remained nearly invariant (12.7 pF and 11 pF for 24 and 48 h, respectively). This could be ascribed to the significant densification, as shown in Fig. 6. Since there was not much grain growth, the matrix compaction led to an increase in the number of grain-boundaries within a unit volume. As the electrical parametric analysis showed the resistance to be mainly grain-boundary dominated, this is reflected by an increase in the overall resistance of the sample with increasing soak time. In addition, the values of the depression angles (10–15°) are similar



(a)



(b)

Figure 6 Microstructural evolution in the $CaSnO_3$ samples sintered at 1350 °C for (a) 24 h and (b) 48 h.

to those obtained in the samples sintered at 1200 °C. This parameter indicates that the degree of homogeneity or heterogeneity of the conducting paths and underlying mechanisms remained uninfluenced by the sintering schedules.

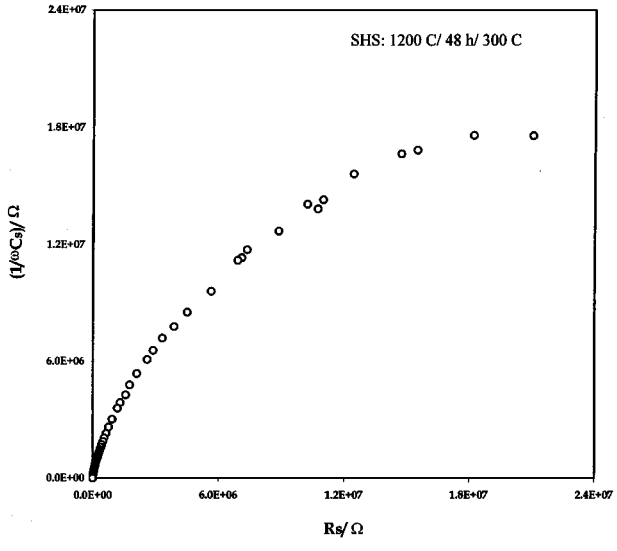
The relaxation features observed in the room-temperature ac data were nearly invariant at higher temperatures as well. This is shown in Fig. 7a to h, which represents the ac data acquired at 300 °C on samples sintered at various temperature-time profiles. The extracted parameters are listed in Table I.

The electrical response of the samples sintered at 1600 °C for 2 h did not show a sharp difference from those exhibited by the samples sintered at lower temperatures. These results are shown in Fig. 8a to c. However, there is a drastic decrease in the total resistance, which is verified as a lumped quantity from a single-like semicircular relaxation in the Z*-plane and overlapped two-like semicircle in the M*-plane. The relaxation in the C*-plane was akin to those observed in previously discussed samples.

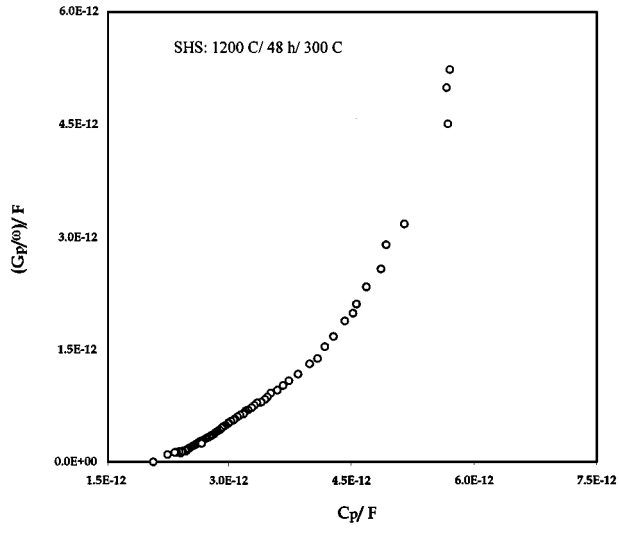
The extracted electrical parameters in this case are as follows: (1) $C_{total} = 8$ pF, $R_{total} = 20.3$ MΩ and $\theta_{total} = 15.8°$ from the Z*-plane; (2) $C_2 = 3.3$ pF, $R_1 = 3.8$ MΩ; $C_{total}(= C_1 + C_2) = 9$ pF and $\theta_g = 10.7°$ from the C*-plane. The low-frequency region of the M*-plot (Fig. 7c) gives $R_{gb} = 14.1$ MΩ, $C_{gb} = 5.6$ pF and $\theta_{gb} = 3.9°$. The depression angles (10–15°), remain similar to those obtained in the samples sintered either at 1200 or 1350 °C.

Significant decrease in the total (dc) resistance is attributed to the decrease in the lumped grain and grain-boundary resistance of the samples sintered at 1600 °C for 2 h. Fig. 9 illustrates the microstructural evidence for this argument. As can be seen, in these samples significantly uniform grain growth (grain size ∼3–5 μm) is achieved through a high degree of densification, thereby obtaining better grain-to-grain connectivity. The material has consistently exhibited higher conductivity of the grains compared to the grain-boundaries. The electrical field falling regions are likely to remain unaltered for all the sintering temperature-time (T–t) profiles.

In order to assess the suitability of the SHS-derived $CaSnO_3$ sintered bodies as low TCC components, the ac electrical data acquired over the temperature range 25–300 °C were also examined by the conventional Bode

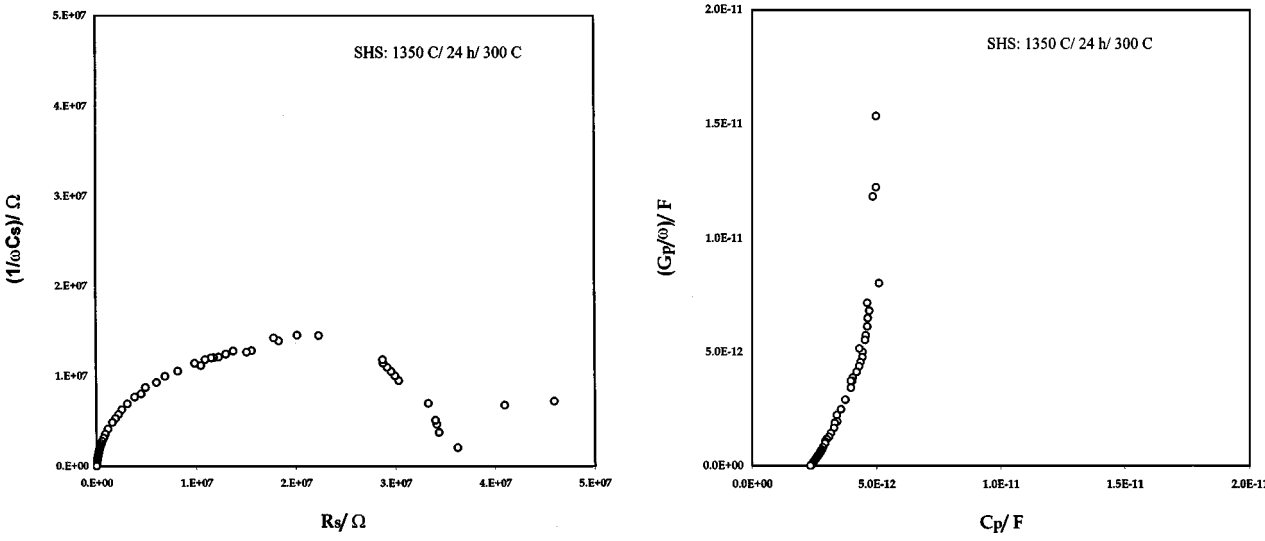


(a)



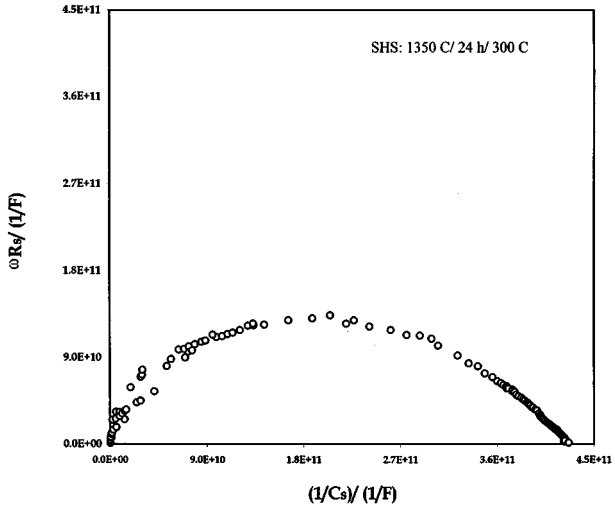
(b)

Figure 7 Relaxation of the ac data acquired at 300 °C on $CaSnO_3$ samples sintered with different T–t profiles.

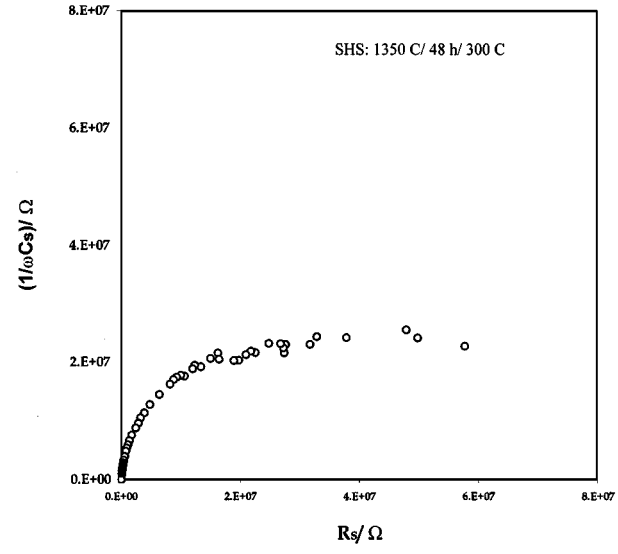


(c)

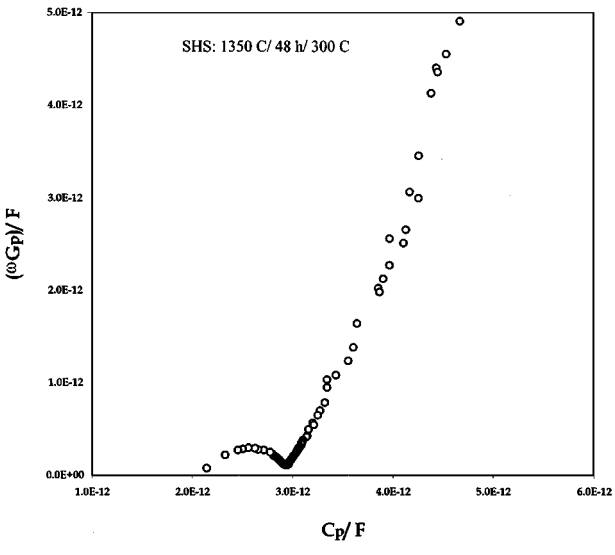
(d)



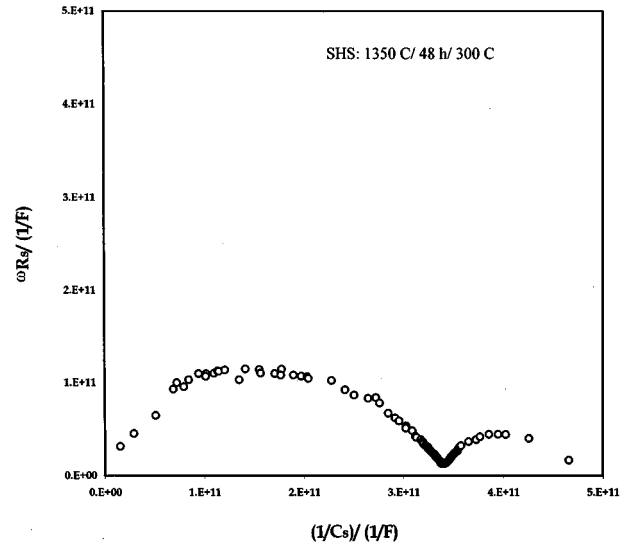
(e)



(f)



(g)



(h)

Figure 7 (Continued).

plot formalism [7–10]. Since the extracted information coincided with the results obtained in the complex plane formalisms (as demonstrated above), these Bode plots are not presented. Some features of the Bode plots can be summarized as: (i) the sample capacitance remains invariant with frequency over a wide range both at room and elevated temperatures up to 300 °C, (ii) in the same range of frequency the capacitance also remained nearly invariant as the soak time increased, and (iii) the average magnitude of capacitance in this temperature

TABLE I Circuit parameters extracted from the relaxations in the impedance, complex capacitance and modulus planes shown in Fig. 7 for $CaSnO_3$ at 300 °C

Sintering profile	Plane	Circuit parameter
1200 °C/ 48 h	Impedance	$R_{total} = 49.6$ MΩ ($R_{dc} = 50$ MΩ) $C_{total} = 6.65$ pF $\theta_{total} = 17.6°$
	Complex capacitance	C_3 (extreme left finite intercept) = 2.44 pF
		$C_3 + C_2$ (relaxation in intermediate frequency domain) = 3.08 pF
		$C_1 + C_2 + C_3 = C_{dc} = 6$ pF $C_2 = 0.64$ pF $R_2 = 1.3$ MΩ $\theta_2 = 3.1°$ $C_1 = 2.92$ pF
1350 °C/ 24 h	Impedance	$R_{total} = 43.3$ MΩ $C_{total} = 5.5$ pF $\theta_{total} = 22.6°$
	Complex capacitance	C_2 (extreme left finite intercept) = 2.35 pF $C_1 + C_2 = C_{dc} = 5$ pF
1350 °C/48 h	Impedance	$R_{total} = 69.7$ MΩ ($R_{dc} = 66.7$ MΩ) $C_{total} = 5$ pF $\theta_{total} = 13.2°$
	Complex capacitance	C_2 (extreme left finite intercept) = 2.2 pF
		$C_3 + C_2$ (semicircular relaxation at intermediate frequency domain) = 3 pF
		$C_1 + C_2 + C_3 = C_{dc} = 5$ pF $C_2 = 0.8$ pF $R_2 = 42.6$ kΩ $\theta_2 = 17.7°$ $C_1 = 2$ pF
	Modulus	Low frequency regime: $R'_m = 66.63$ MΩ ($\approx R_{total} \approx R_{dc}$) $C'_{gm} = 2.9$ pF

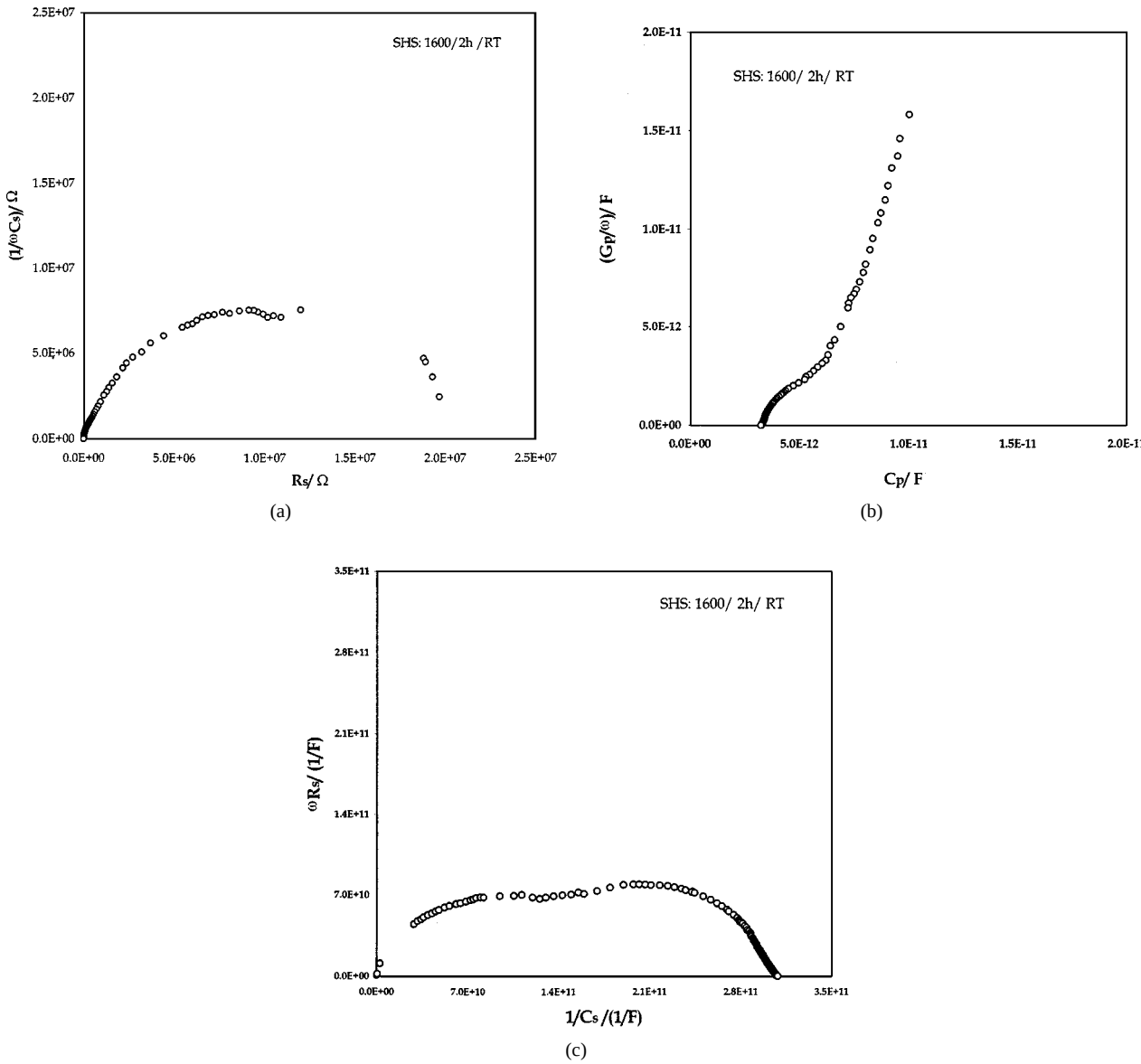


Figure 8 Room temperature complex plane plots for the samples sintered at 1600 °C for 2 h. (a) Impedance (Z*) plot. (b) complex capacitance (C*) plot, and (c) modulus (M*) plot of the same data.

range was nearly unaffected (a few pF) for the samples sintered at 1200, 1350 and/or 1600 °C for durations between 2 and 48 h.

The foregoing features are in contrast to the observations reported by Mandal *et al*. [3], where a strong frequency-dependence of capacitance was observed at arbitrarily selected spot frequencies (1, 10, and 100 kHz). The capacitance is essentially the terminal capacitance resulting from a single-stage sintering schedule and remained frequency dependent. Moreover, the circuit element(s) operative within these samples were not examined. Their results might have had

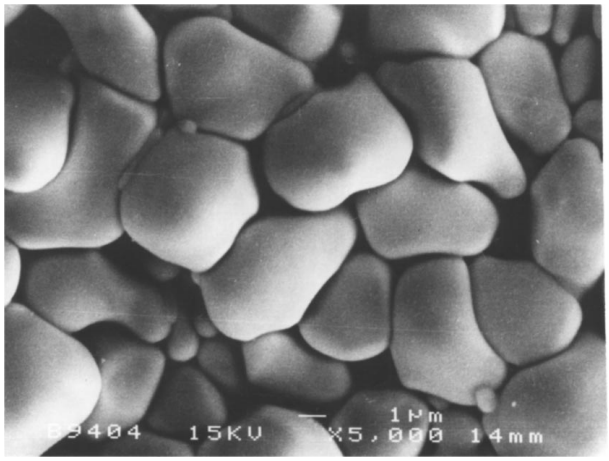


Figure 9 Microstructural features of the $CaSnO_3$ samples sintered at 1600 °C for 2 h.

different microstructural development which caused frequency-dependent trapping states within the electric field falling regions. Such a feature is sensitive to variable processing methods and is likely to be drastically different from that reported here. The fact is that the role of traps seems to have a greater influence on their samples. It is worthwhile mentioning that the ZnO-based varistor materials are heavily dominated by the multifold trapping states at the grain-boundary depletion regions which play a key role in the total electrical characteristics despite a large variation in the sintering and soak time schedules [15]. Strong frequency-dependent behavior has also been documented for these varistors via the complicated Mott-Schottky response [6].

A steep transition in capacitance in the Bode plane as well as dielectric loss tangent as a function of frequency is observed for each of the samples investigated, at the lower end of the measurement frequency range. This consistent response is attributed to a possible polarization effect at the electrode-to-sample interface at these frequencies. The dielectric loss (tan δ) was also found to be too small over several decades of frequency at elevated temperatures. Basically, the capacitance characteristics of the material remained identical in the samples derived via the SHS and the SSR techniques. In the case of SSR-derived samples, the average capacitance value was 2–3 pF and 3–7 pF in bodies sintered at 1200 and 1350 °C, respectively [1]. In this study, an average capacitance value ranging between 2 and 5 pF was obtained for the samples sintered in the temperature range 1200–1600 °C. The nature of the green powder seems to have an influence on the development of microstructure in the sintered bodies. In the case of SHS-derived $CaSnO_3$, there was evidently a restricted grain growth with average grain size of the domain of $\sim$1 μm up to 1350 °C.

This investigation indicates that SHS-derived $CaSnO_3$ material has promising potential as a candidate for use as a capacitor element. It possesses an ultrasmall value of the temperature coefficient of capacitance (TCC), which is summarized in Table II. Development of a benign microstructure with better control over grain size is likely to be responsible for the smaller scatter in the capacitance values when compared to that in SSR-derived $CaSnO_3$ samples.

TABLE II Summary of the TCC values for SSR- and SHS-derived $CaSnO_3$ in the temperature range 25–300 °C

Synthesis technique	Sintering (T–t) profile	TCC (K^{-1})[a]
SSR	1200 °C/ 24 h	$+1.5 \times 10^{-4}$
SSR	1200 °C/ 36 h	-2.1×10^{-3}
SSR	1200 °C/ 48 h	-1.7×10^{-3}
SSR	1350 °C/ 24 h	-1.5×10^{-3}
SSR	1350 °C/ 48 h	-2.6×10^{-3}
SHS	1200 °C/ 12 h	-1.2×10^{-3}
SHS	1200 °C/ 24 h	-1.3×10^{-3}
SHS	1200 °C/ 48 h	$+1.5 \times 10^{-4}$
SHS	1350 °C/ 24 h	-2.6×10^{-3}
SHS	1350 °C/ 36 h	-2.3×10^{-3}
SHS	1350 °C/ 48 h	-3.4×10^{-3}

[a]Herbert [19] defines the temperature coefficient of capacitance (TCC) as: TCC = (1/C) (∂ C/ ∂ T).
Using this definition, and the extracted magnitude of capacitance at various temperatures in the range 25–300 °C, the TCC values listed above were computed.

4. Equivalent circuit model

In the light of the present data-handling criteria a systematic equivalent circuit analog can be developed. The multi-plane analytical technique provided methodical extraction of the circuit elements which can be incorporated in the model. Based on Z*- and M*-plane analyses we can construct a voltage-dividing representation consisting of an R-C parallel configuration. For the lumped single-like relaxation processes a single R-C ($=R_{\text{total}}-C_{\text{total}}$) parallel configuration can be used. Such a lumped parallel combination is a simplistic view of any electrically-active material system. Nevertheless, the R_{total} and C_{total} values indicate a dc condition (i.e. frequency tending to zero) of the device which is shown in Fig. 10(a).

When two overlapped relaxations are present within this lumped configuration, the R_{total}-C_{total} combination can be viewed as two voltage-dividing segments. Each segment consists of an R-C parallel combination. Thus, the parallel combination of R_g-C_g is in series with the parallel combination of R_{gb}-C_{gb}. In this way, the lumped grains and grain-boundaries within the microstructures can be simplified [11, 12]. This is shown in Fig. 10(b).

To develop the equivalent circuit model further by incorporating the role of trapping states within the grain-boundary regions (particularly in the electric field falling regions), a current-dividing configuration can be postulated. Such a configuration is supported by the C*-plane relaxation. In this case the concept of barrier-layer (grain-boundary depletion contribution and single-crystal-like bulk dielectric response) capacitance can be used. This is in parallel with the trapping response. A trapping response is a series R-C combination [6]. The barrier-layer capacitance, trapping response, and the dc resistance can be put together to form a current-dividing circuit, which is shown in Fig. 10(c).

The multiple representation of the equivalent circuit model provided in Fig. 10 ultimately reduces to a singular (unified) nature of the total conduction across the sample (between the electrodes). Thus, a single equivalent circuit model can be visualized for the unknown device under test (DUT) depending on the investigator's

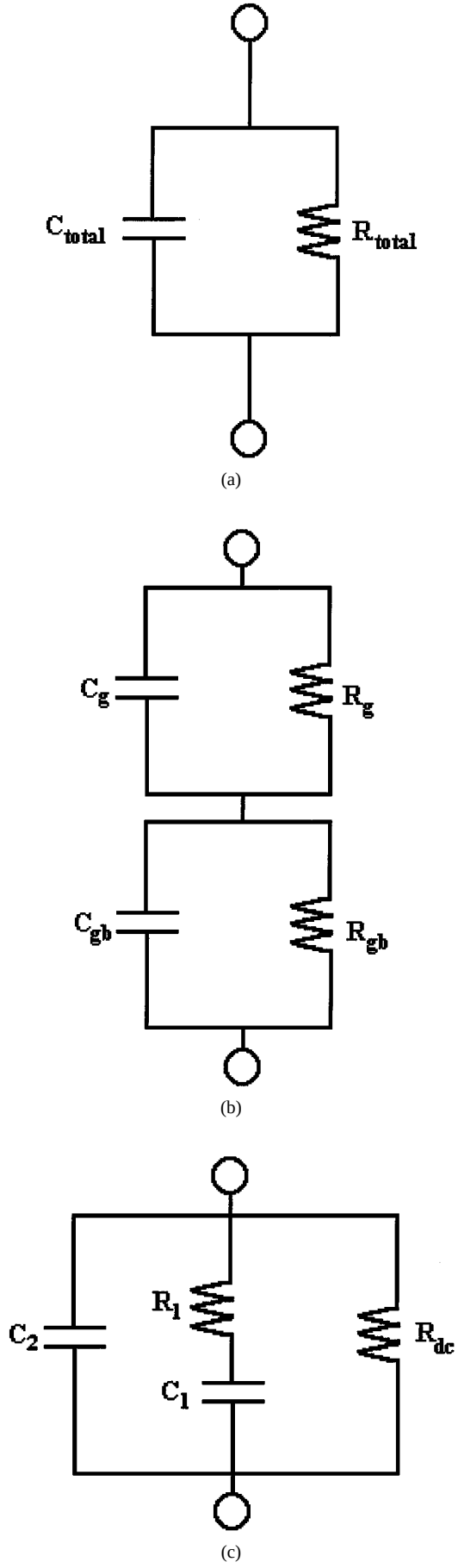


Figure 10 (a) Equivalent circuit model corresponding to the elements extracted in the Z^*- and M^*-plane analyses, (b) a lumped equivalent circuit model for the single-like relaxation and (c) an equivalent circuit showing trapping response at the grain-boundary depletion regions obtained in the C^*-plane.

conceptual perspective and understanding. To illustrate the meaning of this situation further, it is reasonable to reduce multiple configuration of the equivalent circuit model of Fig. 10 to a single equivalent circuit model based on the investigator's emphasis on the extracted parameters including probing to an in-depth profile of the contributing elements constituting each of these equivalent circuit models. Therefore an unknown DUT or a material system when examined, thus, ascertains the application criteria based on the evaluation of the extracted parameters obtained from each of these equivalent circuits resulting from the approaches of the choices of the analytical methods. Nevertheless, a complete evaluation of each of the extracted parameters from each of these equivalent circuit models provides a broader perspective as far as potential application of the unknown DUT or the material system. In this way the equivalent circuit models contained in Fig. 10 are interchangeable, and as such any one of them is representable depending on the experimental facilities (or limitations) and an investigator's attitude. The experimental limitation, capability, visibility, window of investigation, non-equilibrium variables, etc. will allow the ultimate choice of the equivalent circuit model. It is relevant to emphasize multiple representation of the equivalent circuit for the same DUT that converges to a single equivalent circuit configuration when the underlying contributing elements are physically located, and comprehended of their purpose as a contributing element emerging from a specific behavior within the DUT.

5. Conclusions

The concurrent multi-plane (Z^*, C^* and M^*) analytical approach has been employed to elucidate the underlying operative mechanisms in the $CaSnO_3$ material system. This material system is synthesized via a novel self-heat-sustained reaction technique. The lumped parameter/complex plane analysis technique provided a meaningful solution to the underlying competing phenomena within the microstructures. The results were further supported by the Bode plots. Overall, the way ac electrical data have been handled, analysed, and parameters extracted to understand their role within the microstructures has provided a broader aspect of the immittance spectroscopy. Such in-depth investigation as well as the development of the equivalent circuit model in various situations provide an insight about the material behavior.

This investigation reveals that $CaSnO_3$ can be used as a capacitor material due to its capacitance invariance in the large frequency domain. Also this material system possesses an ultra-small temperature coefficient of capacitance. The sintering temperature (1200–1600 °C) and soak time (2–48 h) profiles allowed us to understand the processing conditions via the kinetics pertaining to the novel self-heat-sustained reaction technique. These kinetics helped to determine the functional behavior of $CaSnO_3$ and its selectivity as a capacitor element. The nearly uniformly distributed small grain size ($\sim$1 μm) in samples sintered up to 1350 °C and uniform

grain growth (average grain size ~3–5 μm) in samples sintered at 1600 °C (soak time 2 h) are the controlling factors for the resulting electrical characteristics. It is emphasized that densification plays a key role in achieving a steady invariant capacitance and ultra-low TCC for this material. The minute difference in the bulk dielectric behavior is attributed to the minor adjustment in the formation of the grain-to-grain contact region. The trapping parameters are believed to be less sensitive to the resulting dielectric as a capacitor element.

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